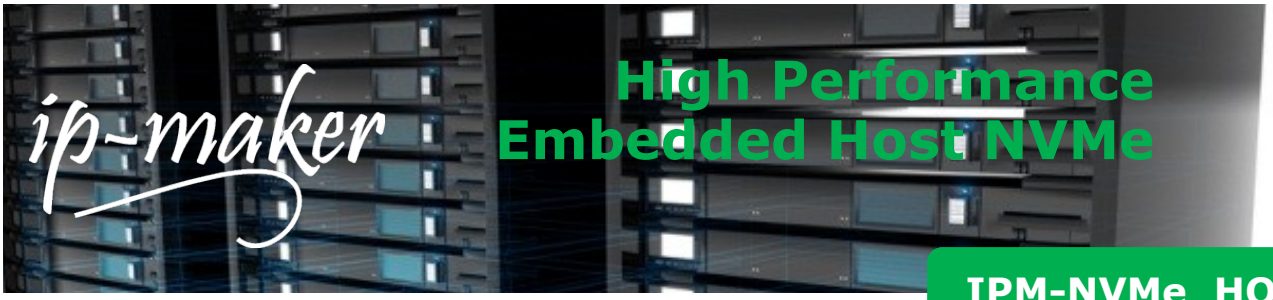


High Performance Embedded Host NVMe

IPM-NVMe_HOST

Host NVM Express

Key Features

- Automatic PCIe/NVMe init
- RAM or AXI4 or Avalon interface
- Scalable architecture
- Options:
  - OPAL 2.0 management
  - NVMe multi-queue management

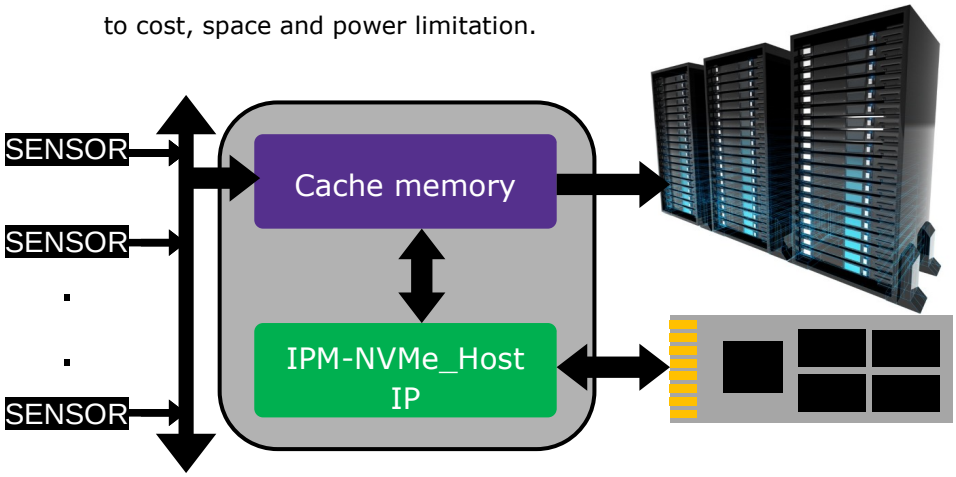
Benefits

- Ultra low latency
- Very high throughput
- Low gate count
- No need of CPU
- No specific knowledge required

Overview

The IPM-NVMe_Host core is a verilog IP to be integrated in a FPGA or ASIC design. It fully manages the NVMe and PCIe protocol on the host side without requiring any CPU and any specific knowledge. It can be used with any NVMe SSD available on the market, or with a custom design based on the IPM-NVMe_Device IP from IP-Maker.

The IPM-NVMe_Host is well suited for embedded applications requiring a high throughput storage such as recorder and video applications. 1+ million IOPS performance requires the use of an expensive CPU, which is not feasible in an embedded system due to cost, space and power limitation.



Deliverables

- Verilog RTL source code
- Example design
- Synthesis scripts
- Technical documentation
- Technical support

Using the pre-validated IPM-NVMe_Host IP core greatly reduces time-to-market for storage OEM; this allows the OEM to benefit from a powerful data transfer manager. The IPM-NVMe_Host IP core is full featured and easy to use with multiple application interface such as AXI or RAM-like.

As the first NVMe IP core supplier, IP-Maker's experience regarding NVMe's development is unmatched. Moreover, it provides the IPM-NVMe_Device controller for data storage applications, such as NVMe SSD and NVMe NVRAM.

nvm EXPRESS

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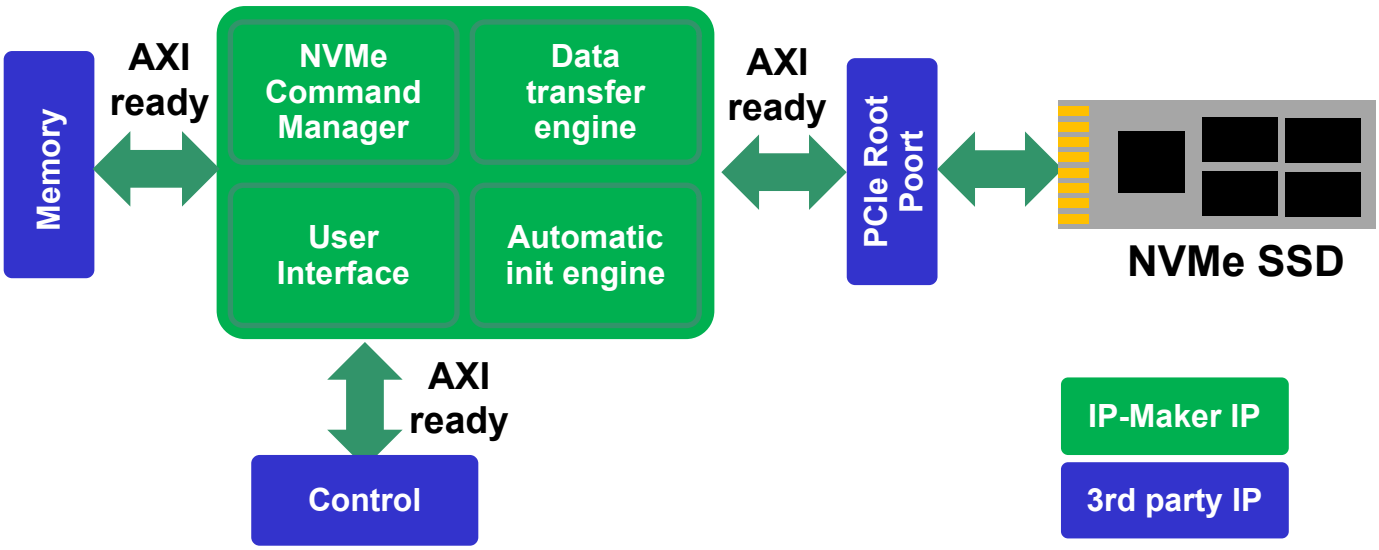
ip-maker

IPM-NVMe_HOST

Description



The architecture of the IPM-NVMe_Host IP is based on 4 main blocks:

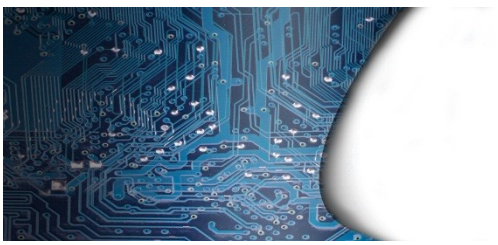
- Automatic init engine: PCIe and NVMe device initialization, hardware discovering
- User Interface: memory configuration and input for the transfer request by the API
- NVMe command manager: translation of the data request from API into a NVMe command.
- Data Transfer Engine: management of the data transfer between the NVMe SSD and the memory

It delivers very low latency since it is a full hardware host NVMe implementation. That takes only few dozens of clock cycles (compared to multiple thousands of clock cycles for a software NVMe driver on a CPU). In addition, there is no needs of PCIe interrupt management because it is directly processed by the Host NVMe manager, therefore avoiding context switches.

Reference design

The IPM-NVMe_Host IP is available for evaluation and demo using a reference design based on a Xilinx FPGA boards attached to a M.2 NVMe SSD. It embeds a testbench allowing to configure the IO access : IO size, random/sequential, read/write…

Performance results: it reaches up to 3,4GB/s, which is the limitation of the SSD used (Gen3x4 NVMe SSD specification max = 3,4GB/s).



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