Data protection ECC

IPM-LDPC

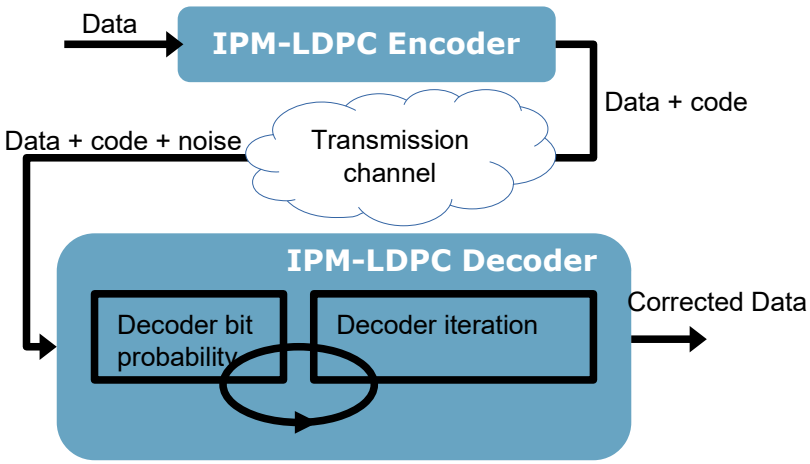
LDPC Encoder/ Decoder IP core

Key Features

- IPM-LDPC for NandFlash Storage
  - Adaptable BER
  - Up to 6 checks per bit
  - Customizable data path
- IPM-LDPC for short code
  - Option to be full asynchronous
  - Option to be in 3 clock cycles
- Fully Configurable
  - Matrix generator
  - Datapath
  - Number of iteration checks
  - Block size

Overview

Nand Flash write cycles are limited. An ECC detects and corrects failed operations, increasing the lifetime of the Nand Flash memory. For Nand Flash-based data storage, using an ECC is mandatory to ensure data validity. IP-Maker's powerful IPM-LDPC is based on the LDPC algorithm. The IP-Maker IPM-LDPC Encoder/Decoder is full-featured with multiple parameters to fit your own needs in FPGA and SoC designs. In fact IPM-LDPC Encoder/Decoder is fully configurable, allowing to it reach the best latency or the smallest footprint. Customizable parameters include: number of check per bit, number per iteration, block size, bit error rate ….



Benefits

- Full hardware
- High performance / low latency
- Low gate count

Deliverables

- Verilog RTL source code
- Simulation environment
- Technical documentation
- Technical support

For design that uses shorter packets and codes, a subset of our prevalidated and improved IPM-LDPC is available to protect your private datas.

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