Data protection ECC

IPM-BCH

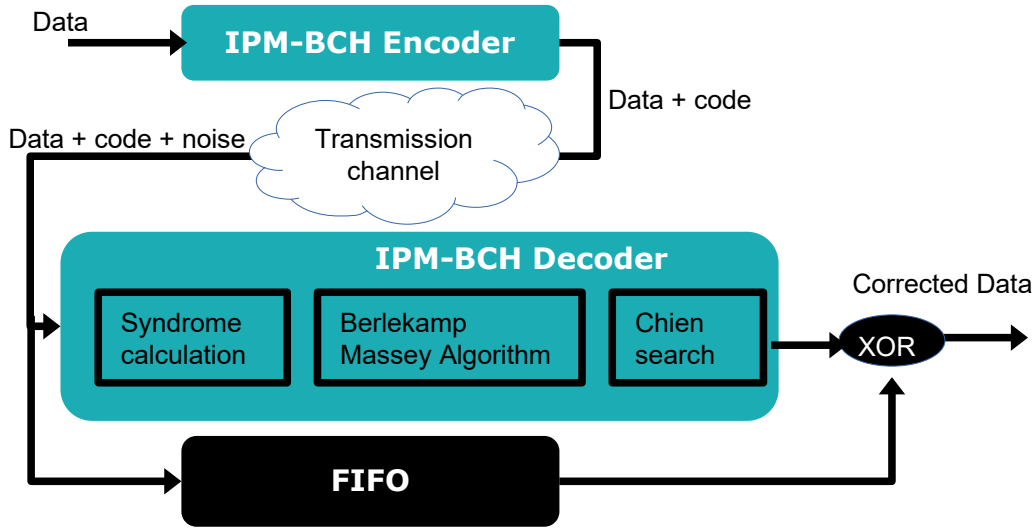
BCH Encoder/ Decoder IP core

Key Features

- IPM-BCH for NandFlash Storage
  - Up to 84 error-bits/block
  - Configurable block size
- IPM-BCH for short code
  - Option to be full asynchronous
  - Option to be in 3 clock cycles
- Fully Configurable
  - Latency
  - Datapath
  - Error number
  - Packet size

Overview

Nand Flash write cycles are limited. An ECC detects and corrects failed operations, increasing the lifetime of the Nand Flash memory. For Nand Flash-based data storage, using an ECC is mandatory to ensure data validity. IP-Maker's powerful IPM-BCH is based on the BCH algorithm. The IP-Maker BCH Encoder/Decoder is full-featured with multiple parameters to fit your own needs in FPGA and SoC designs. In fact IPM-BCH Encoder/Decoder is fully configurable, allowing to it reach the best latency or the smallest footprint. Customizable parameters include: Chien Search algorithm, Galois Field, and data path.



Benefits

- Full hardware
- performance/gatecount
- All Galois fields

Deliverables

- Verilog RTL source code
- Simulation environment
- Technical documentation
- Technical support

For design that uses shorter packets and codes, a subset of our prevalidated and improved IPM-BCH is available to protect your private datas.

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