Data Transmission ECC

IPM-ECC

BCH Encoder/Decoder IP Core

Key Features

- DVB-S2 ECC
  - Up to 12 errors
  - Short and Normal frames
- Fully Configurable
  - Latency
  - Datapath
  - Error number
  - Packet size

Benefits

- Full hardware implementation for the best performance: encoding, error detection and correction
- All Galois fields covered
- Best performance / gatecount tradeoff reachable
- Reduced Time-To-Market by using validated IP

Evaluation

- Full features
- Simulation testbench
- Evaluation package for FPGA

Deliverables

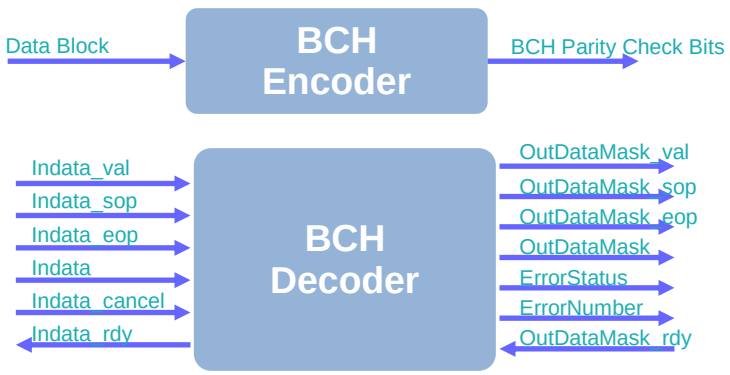
- Verilog RTL source code
- Synthesis scripts
- Technical documentation
- Technical support

Overview

Data transmission, such as satellite communication and digital video broadcasting, may be have datan errors. Therefore, a detection/correction code is required. BCH code is used in DVB-S2. IP-Maker developed a BCH Encoder/Decoder, full featured, easy to use into FPGA and SoC designs.

ECC BCH Decoder in a data transmission system

The IP-Maker BCH Encoder/Decoder is fully configurable, allowing to reach the best latency or the smallest footprint. The IP-Maker BCH Encoder/Decoder IP Core is delivered in Verilog RTL that can be implemented in an ASIC or FPGA. It is fully tested with test benche models and hardware tested with FPGAs. The package includes verilog RTL code, technical documentation, and complete test environment.



BCH Encoder / Decoder Overview

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