

SSD Reference Design

Services

- ↪ IP customization & integration
- ↪ Board design
- ↪ Low level software

Benefits

- ↪ Fast prototype design
- ↪ Low cost proof of concept
- ↪ State of the art storage device

Deliverables

- ↪ Prototype with source code
- ↪ Schematics
- ↪ Technical documentation, support

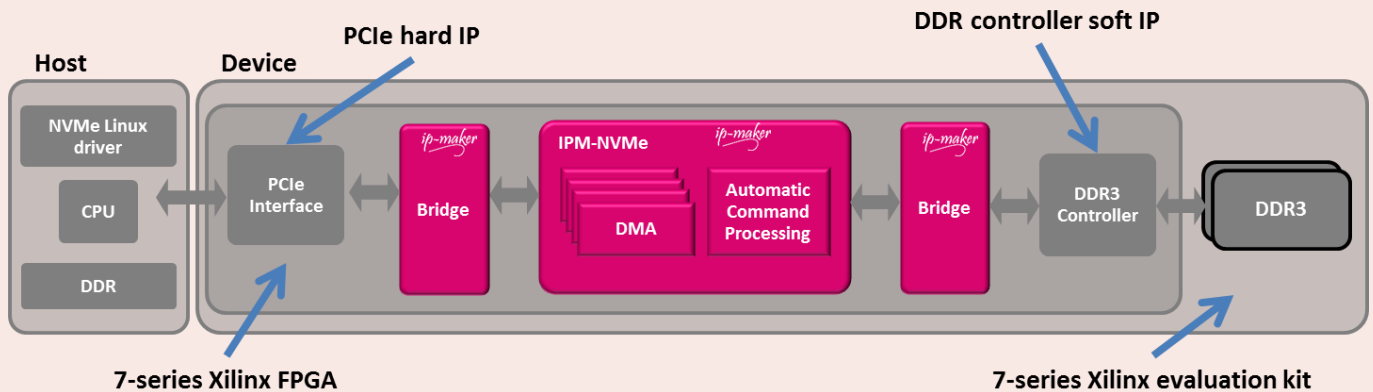
Overview

In addition to IP core design (NVM Express, Universal NANDflash controller and ECC), IP-Maker is able to provide full design services including IP integration, IP customization and board design. The combination of the expertise in storage-specific IP cores and storage system design makes IP-Maker the ideal partner for a state of the art SSD reference design.

Such reference designs are perfect for new non-volatile memory technology that come with very high density or very high data transfer rate memory (such as MRAM, RRAM...). IP-Maker can help in designing an optimized and dedicated controller for a high performance storage system (NVMe PCIe SSD). This is an easy and low cost path for a proof of concept as a new high performance technology demonstrator or as a market tester

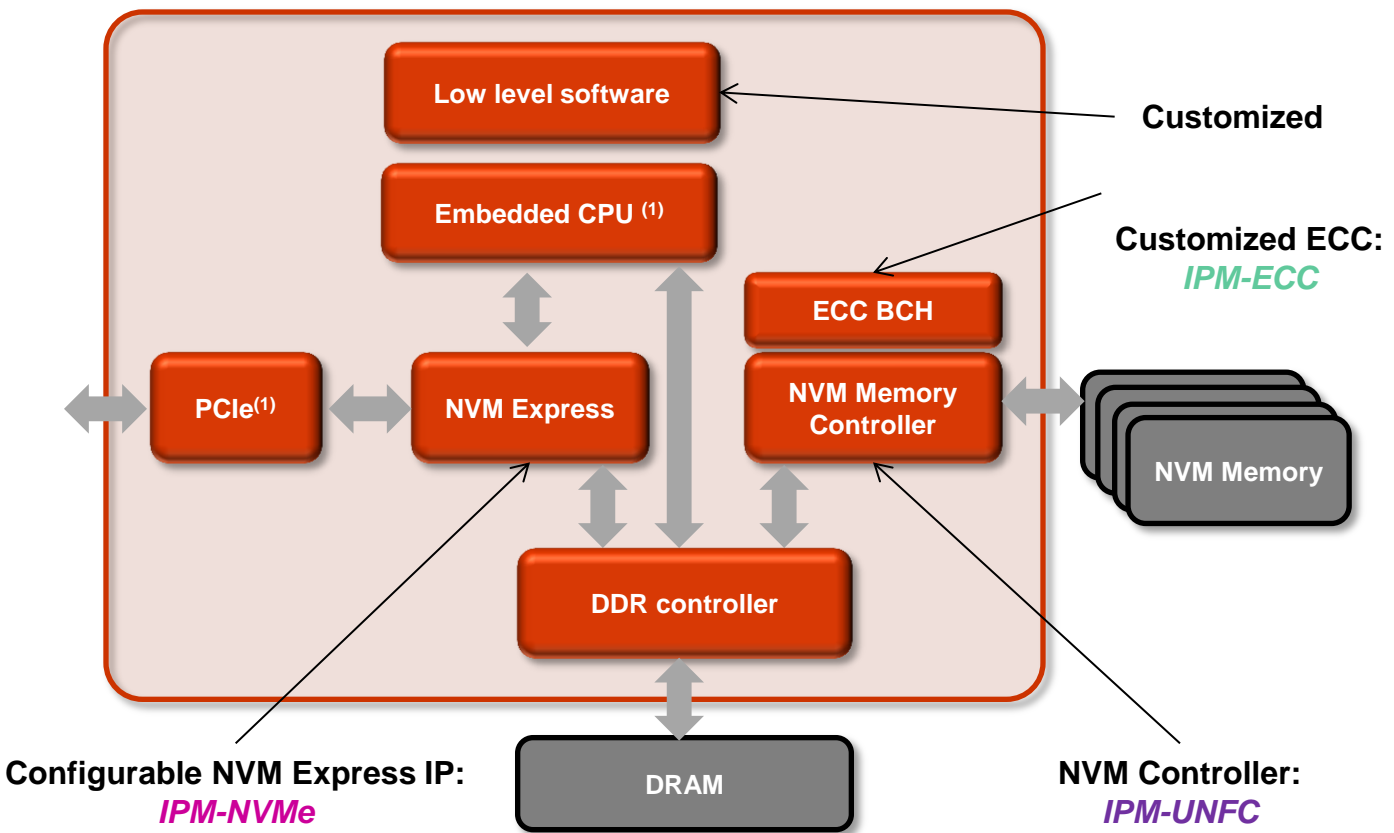
Low latency NVMe reference design

The NVMe reference design below is available on Xilinx FPGAs. It comes with a PCIe Gen 2x4 (FPGA hard IP). On the other side, the NVMe is connected to the DDR3 controller (soft IP). All the NVMe management is done by the full hardware NVMe IP, therefore avoiding the use of embedded processor. It delivers high performances such as about **10µs** latency and **350kIOPS**.



Typical reference design

Below is a typical PCIe-based reference design realized on a FPGA-based board. The IP-Maker NVM Express IP core (IPM-NVMe) is integrated in the FPGA with connections to the PCI Express controller, the embedded 32bit processor and the DRAM controller. The IP-Maker NandFlash controller (IPM-UNFC) is integrated with the IP-Maker ECC (IPM-ECC) and is connected to the onboard NandFlash memories. Embedded low level software and NVM Express drivers are adapted according to the customer specifications.



(1) From third parties or FPGA vendors



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