High Performance Solution for PCIe SSD

IPM-NVMe

NVM Express compliant

Key Features

- NVM Express Compliant
- Automatic Command Processing
- Multi-Channel DMA
- Up to 65536 I/O queues
- Weighted round robin queue arbitration support
- All commands/log management
- Legacy interrupt/MSI/MSI-X support
- Full NVMe registers support
- Asynchronous event management
- Low Power architecture

Benefits

- UNH-IOL NVM Express certified
- Ultra low latency
- Very high throughput
- Low power architecture
- Low gate count
- Cost reduction thanks to interface standardization
- Validated IP reduces time to-market

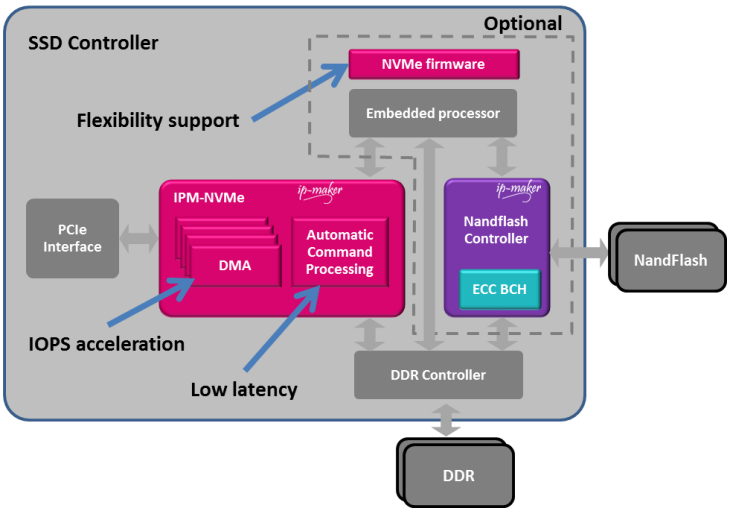
Deliverables

- Verilog RTL source code
- Low level firmware
- Synthesis scripts
- Technical documentation
- Technical support

Overview

Typical storage controllers are composed of a communication interface and a Nandflash controller. In this case, all the data flow is managed by the external host processor. However, this architecture cannot sustain high performance applications. The NVMe IP core designed by IP-Maker is a powerful data transfer manager integrated into the PCIe SSD Controller between the communication interface and the Nandflash controller, therefore off-loading the host CPU.

The IP-Maker NVMe IP is UNH-IOL NVM Express compliant. It is part of the official NVMe integrator's list: https://www.iol.unh.edu/registry/nvme

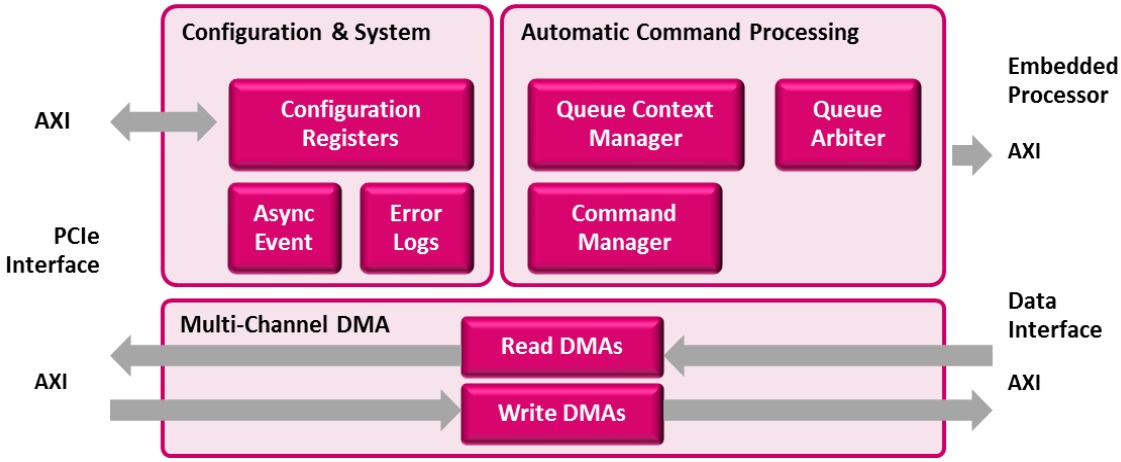


High-performance PCIe SSD Controller Architecture

Server manufacturers benefit from driver standardization. All PCIe SSDs NVM Express-compliant support a unique driver providing ease-of-use and cost-reduced software development.

The IP-Maker NVMe IP core is fully-featured and easy to use in FPGA and SoC designs. The full hardware architecture, which is gates number optimized, provides a power efficient IOPS rate, leading to low power SSD controller capabilities.

IP-Maker is NVM Express contributor

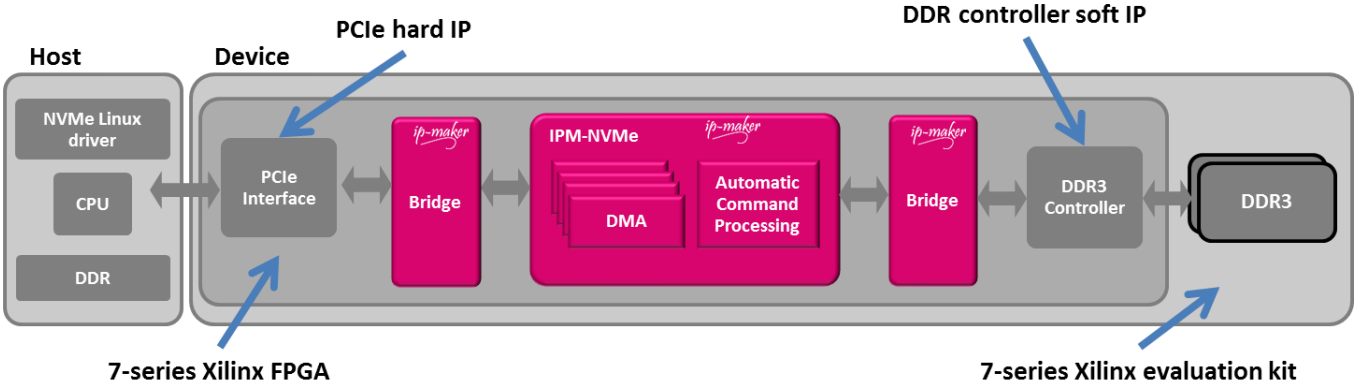


Description

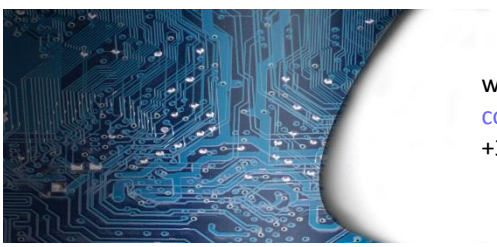
The complete NVMe system is managed by a submission and a completion administration queue (activation of others queues, arbitration rules, request of log, attribution of events….).
All queues are managed independently, the system is very flexible and allows users to attribute dedicated queue to a specific action. To add service quality, a set of arbitrations are available: either a simple round robin or a weighted round robin. There is also the capability of executing a configurable number of commands on a queue before a new arbitration.
All available memories (cache buffers of page size) are signaled to the system by the status memory bus. The memory bus dispatcher dynamically allocates buffers to submission queues. All commands executed by the differing submission queues are sent to the embedded processor with the allocated buffer allowing interaction with a third-party system.

Reference Design

The NVMe IP can be used in both ASIC and FPGA. It has been ported and validated on the Xilinx 7-series FPGAs. For evaluation and demonstration purpose, the following reference design is available using the Zynq development kit ZC706 from Xilinx.



Performance: this reference design achieves **11µs** latency and **350 kIOPS** with the following configuration: PCIe Gen2 x4, QD=4, IO=4kB.



www.ip-maker.com
contact@ip-maker.com
+33 972 366 513

IP-Maker
Les Néréides; 55 rue Pythagore
13290 Aix en Provence
France