High Performance Embedded Host NVMe

Easy NVMe HOST

Host NVM Express

Key Features

- NVM Express Compliant
- Automatic NVMe Command management
- Automatic PCIe/NVMe init
- Single I/O queue
- Single Namespace
- Up to PCIe Gen 3x8

Benefits

- Ultra low latency
- Very high throughput
- Low power architecture
- Low gate count
- No need of CPU
- Reduced time-to-market

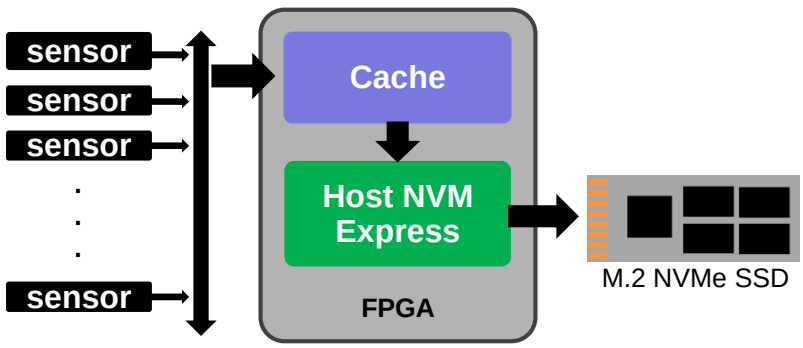
Deliverables

- Verilog RTL source code
- Low level firmware
- Synthesis scripts
- Technical documentation
- Technical support

Overview

The IPM Host NVMe is a verilog IP to be integrated in a FPGA. It fully manages the NVMe protocol on the host side without requiring any CPU. It can be used with any NVMe SSD available on the market, or with a custom design based on the NVMe Device IP from IP-Maker.

The Host NVMe is well suited for embedded applications requiring a high throughput storage such as recorder and video applications. 1+ million IOPS performance requires the use of an expensive CPU, which is not feasible in an embedded system due to cost, space and power limitation.



Using the pre-validated NVMe Host IP core greatly reduces time-to-market for storage OEM; this allows the OEM to benefit from a powerful data transfer manager. The IP-Maker Host NVMe IP core is full featured and easy to use in FPGA designs.

IP-Maker is an active contributor to the NVMe specification and also provides the NVMe device controller for data storage applications, such as NVMe SSD and NVMe NVRAM.

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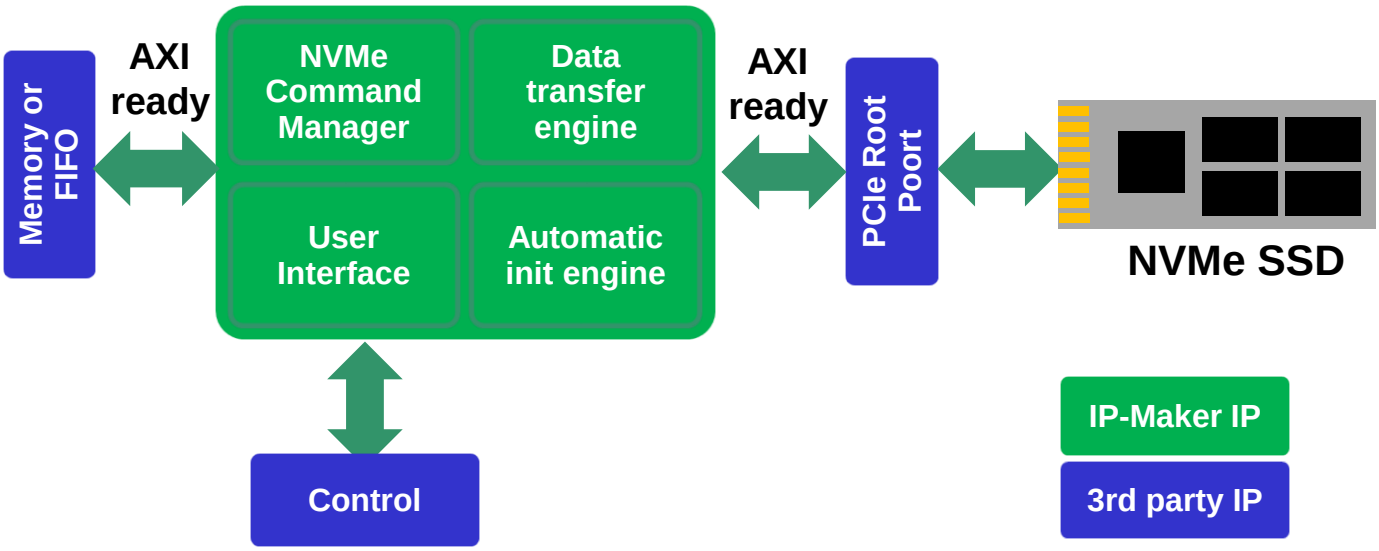
IPM-Host-NVMe

Description



The architecture of the IP-Maker Host NVM Express IP is based on an AXI interconnect. It requires a simple engine (embedded CPU or FSM) for the configuration:

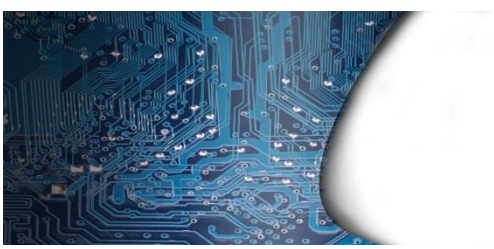
- PCIe and NVMe device initialization
- Hardware discovering
- Shared memory parameters setup

The data from the input (sensor, camera…) are stored in a local shared memory (host caching) such as SRAM or external DRAM. The NVMe command manager dispatches the data flow entry and generates the associated NVMe commands. It also manages the submissions and completion pointers to verify if the submission has been correctly executed.

It delivers very low latency since it is a full hardware host NVMe implementation. That takes only few dozens of clock cycles (compared to multiple thousands of clock cycles for a software NVMe driver on a CPU). In addition, there is no needs of PCIe interrupt management because it is directly processed by the Host NVMe manager, therefore avoiding context switches.

Reference design

A reference design is available on a Xilinx Ultrascale FPGA, using a Samsung M.2 NVMe SSD, reaching up to 3GB/s.



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