Universal NandFlash Controller

IPM-UNFC for Arria 10

UNFC IP Core

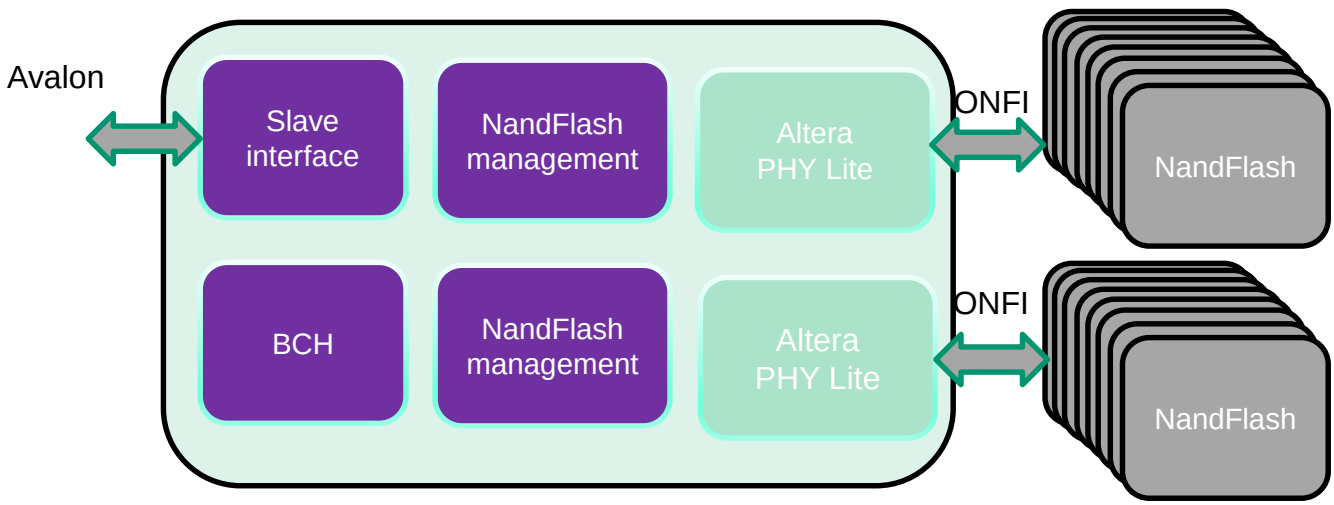
Key Features

- ONFI 4.x Compliant
- SLC / MLC / TLC
- SDR modes 0 to 5
- NVDDR modes 0 to 5
- NVDDR-2 modes 0 to 8
- NVDDR-3 modes 0 to 10
- Avalon interface
- Up to ECC 76-errors / 1k block
- Configurable Data block size

Overview

IP-Maker's Universal NAND Flash Controller (UNFC) IP core is designed specifically to enable commodity Flash memory to be effectively used in enterprise storage applications requiring high reliability and large interconnect bandwidth. Using the pre-validated UNFC IP allows greatly reduced time-to-market for storage OEMs desiring higher IOPS benefitting from lower cost SLC, MLC & TLC NandFlash memory.

The IP-Maker UNFC is full-featured, easy to use in Arria 10 FPGA designs with pre-integrated Aria PHY-Lite interface and an Avalon backend.



Deliverables

- Verilog RTL source code
- Synthesis scripts
- Simulation testbench
- Technical documentation
- Technical support

The NAND flash interface handles all the hardware compliant process (command, address and data sequences). It is ONFI 4.x compliant.

Thanks to the configurable data block size, Data and Metadata can be protected by the ECC. For instance 1024 bytes + x metadata bytes.

Storage ECC

IPM-ECC

BCH Encoder/Decoder IP Core

Key Features

- ECC for NandFlash Storage
  - Up to 76 error-bits/block
  - Up to 1024 bytes block size
- Fully Configurable
  - Latency
  - Datapath
  - Error number
  - Packet size

Benefits

- Full hardware implementation for maximum performance, encoding, error detection and correction
- Balanced performance/gatecount
- All Galois fields covered
- Validated IP reduces Time-To-Market

Evaluation

- Full features
- Simulation testbench
- Evaluation package for FPGA

Deliverables

- Verilog RTL source code
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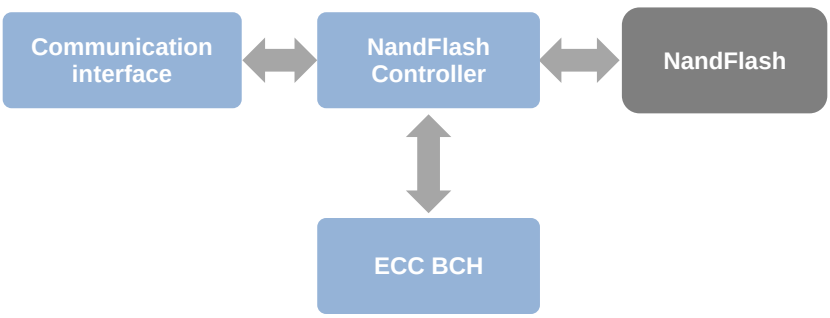
- Technical documentation
- Technical support

Overview

Nand Flash write cycles are limited. An ECC detects and corrects failed operations, increasing the lifetime of the Nand Flash memory. For Nand Flash-based data storage, using an ECC is mandatory to ensuring data validity. IP-Maker's powerful ECC is based on the BCH algorithm. The IP-Maker BCH Encoder/Decoder is full-featured with ease-of-use in FPGA and SoC designs.



ECC BCH in a storage system

The IP-Maker BCH Encoder/Decoder is fully configurable, allowing it to reach the best latency or the smallest footprint. Customizable parameters include: Chien Search algorithm, Galois Field, and data path. The IP-Maker BCH Encoder/Decoder IP Core is delivered in Verilog RTL that can be implemented in an ASIC or FPGA. It is fully tested with test bench models and hardware tested with FPGAs. The package includes Verilog RTL code, technical documentation, and a complete test environment.

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